conductive members buried in a plurality of through holes that go through the first semiconductor chip; and

a plurality of second connecting terminals arranged on a back surface side of the semiconductor element formation surface in the first semiconductor chip, and connected electrically to the semiconductor element via the conductive members,

wherein at least either the first connecting terminals or the second connecting terminals is coupled to a assembly board, and

one of the first connecting terminals and the second connecting terminals are arranged to be facing to the assembly board and the average density of arrangement of the one of the first connecting terminals and the second connecting terminals is lower than that of another of the first connecting terminals and the second connecting terminals.

19. (Amended) A semiconductor device according to claim 12, wherein said at least a portion of the plurality of connecting terminals comprises conductive bumps.

20. (Amended) A semiconductor device comprising:

a first semiconductor chip where a semiconductor element is formed;

a first connecting terminal arranged on a semiconductor element formation surface side in the first semiconductor chip, and connected electrically to the semiconductor element;

a conductive member buried in a through hole that goes through the first semiconductor chip;

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a second connecting terminal arranged on a back surface side of the semiconductor element formation surface in the first semiconductor chip, and connected electrically to the semiconductor element via the conductive member;

a second semiconductor chip stacked on the first semiconductor chip;

a third connecting terminal arranged on a semiconductor element formation surface side in the second semiconductor chip,

wherein one of the first connecting terminal and the second connecting terminal of the first semiconductor chip is arranged at a position facing to the third connecting terminal of the second semiconductor chip, the first semiconductor chip and the second semiconductor chip are electrically connected with each other through the facing connecting terminals,

the second semiconductor chip is thicker or larger than the first semiconductor chip, and

one of the first connecting terminals and the second connecting terminals are arranged to be facing to the assembly board and the average density of arrangement of the one of the first connecting terminals and the second connecting terminals is lower than that of another of the first connecting terminals and the second connecting terminals.

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Please add new claims 21-25 as follows:

-- 21. (New) A semiconductor device comprising:

a first semiconductor chip where a semiconductor element is formed;

a plurality of first connecting terminals arranged on a semiconductor element formation surface side in the first semiconductor chip, and connected electrically to the semiconductor element;

conductive members buried in a plurality of through holes that go through the first semiconductor chip; and

a plurality of second connecting terminals arranged on a back surface side of the semiconductor element formation surface in the first semiconductor chip, and connected electrically to the semiconductor element via the conductive members,

wherein at least either the first connecting terminals or the second connecting terminals is coupled to an assembly board, and

a portion of either the first connecting terminals or the second connecting terminals is distributed and arranged on the central area of the semiconductor chip, and power source supply potential or ground potential is to be applied thereto.

= clm 12

22. (New) A semiconductor device according to claim 21, further comprising a second semiconductor chip stacked on the first semiconductor chip, wherein at least portion of the connecting terminals arranged on a stacked surface between the first semiconductor chip and the second semiconductor chip of the first connecting terminals and the second connecting terminals in the first semiconductor chip is coupled to the second semiconductor chip.

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= clm 13

23. (New) A semiconductor device according to claim 21, further comprising a second to an n-th (wherein n is a positive integer of three or more) semiconductor chips stacked above first semiconductor chip, wherein at least portion of the connecting terminals arranged on a stacked surface between the first semiconductor chip and the second semiconductor chip of the first connecting terminals and the second connecting terminals in the first semiconductor chip is coupled to the second to n-th semiconductor chips.

= clm 19

24. (New) A semiconductor device according to claim 22, wherein said at least a portion of the plurality of connecting terminals comprises conductive bumps.

= clm 20 & center location

25. (New) A semiconductor device comprising:

a first semiconductor chip where a semiconductor element is formed;

a first connecting terminal arranged on a semiconductor element formation surface side in the first semiconductor chip, and connected electrically to the semiconductor element;

a conductive member buried in a through hole that goes through the first semiconductor chip;

a second connecting terminal arranged on a back surface side of the semiconductor element formation surface in the first semiconductor chip, and connected electrically to the semiconductor element via the conductive member;

a second semiconductor chip stacked on the first semiconductor chip;

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a third connecting terminal arranged on a semiconductor element formation surface side in the second semiconductor chip,

wherein one of the first connecting terminal and the second connecting terminal of the first semiconductor chip is arranged at a position facing the third connecting terminal of the second semiconductor chip, the first semiconductor chip and the second semiconductor chip are electrically connected with each other through the facing connecting terminals,

the second semiconductor chip is thicker or larger than the first semiconductor chip, and

a portion of either the first connecting terminals or the second connecting terminals is distributed and arranged on the central area of the semiconductor chip, and power source supply potential or ground potential is to be applied thereto. --

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